REMARKS

Priority Document

Applicant submitted the priority document on December 17, 2001. Attached is a return postcard confirming receipt of the priority document by the Patent Office.

Drawings

Applicant submits new formal drawings consistent with those originally filed with the application.

Amendments to specification

Applicant amends the title of the invention as requested by the Examiner.

Section 112 rejections

Applicant amends the claims to provide the necessary antecedent basis.

Section 103 rejection of claim 1

The examiner suggests that in *Cox*[1], the result of lower portion (115) corresponds to "*m* most significant bits of the summation output data value being switched through only the inverted clock signal at the output of the saturation circuit." In Fig. 2, and in column 2, lines 30-44, *Cox* teaches that in a first half-cycle, low order bits are added up and the results are stored in a register 115, and that in a second half-cycle, the remaining high order bits are added up in section 120. At the end of the second half-cycle, all bits S_0-S_3 are stored in the output register 130. The addition of the higher order bits is delayed with respect to the lower bit addition. Nevertheless, the result of the addition is presented at the output *at the same time* for both the higher bits and the lower order bits. A saturation circuit connected to the output of the adder would thus receive all output bits at the same time.

In the present invention the adder ADD forms a summation output data value. The *n–m* least significant data bits are transferred directly to the saturation circuit. This happens when there is a clock signal. The *m* most significant data bits are later switched to the data input of the

[1] *Cox, et al.* U.S. Patent no. 5,010,508.

saturation circuit when an inverted clock signal precedes the clock signal. It is an important feature of the present invention that the last significant data bits are not presented immediately to the saturation circuit. It takes the adder ADD some time until its output state is stable (see page 9 /line 3). As the higher bits of the output data value lead to switching of the saturation circuit they are not presented to the saturation circuit until they are stable. This reduces power loss (see page 2 /lines 3 -27).

Applicant amends claim 1 to clarify that the most significant data bits are transferred to the input of the saturation circuit after the lower significant bits have been transferred. Thus, the claimed subject matter implements a delay for just the most significant data bits. A delay of this type is neither taught nor suggested by the cited art.

Claims 2-7 include the limitations of claim 1 and are allowable for at least the same reasons.

Now pending are claims 1-7, of which claim 1 is independent. No additional fees are believed to be due in connection with the filing of this response. However, to the extent fees are due, or if a refund is forthcoming, please adjust our deposit account 06-1050, referencing attorney docket "12816-026001."

Respectfully submitted,

Date: 6/30/04

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